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2002 SCHEME **EE56**

Fifth Semester B.E. Degree Examination, June-July 2009
Operational Amplifiers and Linear IC'S

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume suitable data wherever required.
3. Use of resistor, capacitor standard values list, Operational Amplifier data sheets are permitted.

1 a. Sketch the circuit of a high input impedance capacitor coupled voltage follower. Briefly explain the circuit operation. Write the design steps. **(08 Marks)**

b. Sketch the circuit of inverting, non-inverting amplifier to set upper out off frequency. Briefly explain. **(08 Marks)**

c. Design a capacitor coupled voltage follower using 741 Operational Amplifier. The lower cut off frequency for the circuit is to be 50 Hz and the load resistance R_L = 3.9 KΩ. I_b max = 500 nA for 741 Operational Amplifier. **(04 Marks)**

2 a. Define slew rate. Discuss the slew rate effect on sinusoidal signal, pulse signal. **(07 Marks)**

b. Calculate the slew rate-limited cutoff frequency for a voltage follower circuit using a 741 Operational Amplifier if the peak of sine wave output is to be 5V. Determine the maximum peak value of the sinusoidal output voltage that will allow the 741 voltage follower circuit to operate at the 800 KHz unity gain cut off frequency given slew rate of 741 Operational Amplifier = 0.5 V/μs **(07 Marks)**

c. Calculate the cutoff frequency limited rise time for a voltage follower circuit using a 741 Operational Amplifier. Also determine the slew rate limited rise time if the output amplitude is to be 5V. Determine the maximum undistorted pulse output amplitude for the 741 voltage follower if the output rise time is not to exceed 1 μs. Calculate the minimum output rise time and the maximum pulse amplitude at that rise time for a 741 amplifier with an upper cut off frequency of 100 KHz. **(06 Marks)**

3 a. Discuss the circuit instability due to stray capacitance in an Operational Amplifier circuit between the inverting, non-inverting input terminals. How to minimize the effects. **(08 Marks)**

b. Sketch the circuit of an inverting amplifier converted to a nonsaturating full wave precision rectifier. Draw the input, output waveforms. Explain the circuit operation. **(07 Marks)**

c. Design a precision full wave rectifier circuit to produce a 2V peak output from a sine wave input with a peak value of 0.5V and a frequency of 1 MHz. Use bipolar operational Amplifier with a supply voltage of ± 15V. For adequate diode current choose I_1 = 500 μA. **(05 Marks)**

4 a. Design an adjustable peak clipping circuit using an inverting operational amplifier to clip at approximately ± (3V to 5V). The circuit is to have unity voltage gain before clipping. Choose I_1 = 2mA. **(05 Marks)**

b. Draw the circuit diagram of an inverting Schmitt trigger using operational amplifier with variable UTP and LTP adjustments. Draw the input, output waveforms. Explain clearly the operation. **(08 Marks)**

c. Explain the working of an operational amplifier based astable multivibrator. Draw the relevant waveforms. **(07 Marks)**

5 a. Sketch the circuit of a triangular / rectangular waveform generator. Draw the output waveforms from the circuit. Explain the circuit operation. **(06 Marks)**

b. Draw the circuit of a phase shift oscillator. Sketch the output and feed back voltage waveform. Explain the circuit operation. **(08 Marks)**

c. Using a 741 operational amplifier with a supply of ± 12V, design a phase shift oscillator to have an output frequency of 3.5 KHz. Choose $I_1 = 50\mu A$. **(06 Marks)**

6 a. Draw the circuits of first order low pass, first order high pass active filters. Sketch the frequency response for each circuit and briefly explain the operation of each filter. **(12 Marks)**

b. Draw the circuit diagram of a single stage band pass filter. **(03 Marks)**

c. Design a single stage band pass filter to have a voltage gain of 1 and a pass band from 300 Hz to 30 KHz. Find quality factor Q and center frequency. **(05 Marks)**

7 a. Define the following performance parameters of a voltage regulator. Line regulation, load regulation, ripple rejection. **(06 Marks)**

b. Draw the circuit diagram of a voltage follower regulator with adjustable output. Discuss the operation. **(07 Marks)**

c. Draw the block diagram representation of PLL and explain. **(07 Marks)**

8 Write short notes on:

a. Sample and Hold circuit

b. Zero crossing detector

c. Universal / state variable active filter

d. Switched capacitor filter. **(20 Marks)**

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